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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,394	12/28/2001	Jum Soo Kim	054216-5016	2075

7590 08/09/2004
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EXAMINER

NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/029,394

Applicant(s)

KIM ET AL.

Examiner

Khiem D Nguyen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-11 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 31st, 2004 has been entered. A new rejection is made as set forth in this Office Action. Claims (7-12) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (U.S. Patent 5,412,600) in view of Osari (U.S. Patent 6,417,086).

In re claim 7, Nakajima discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of: forming a device isolation film in a give region on a semiconductor substrate to define an active region and a device isolation region; defining the active region into a cell region and a peripheral circuit region by a given process; forming a tunnel oxide film (FIG. 23(A): 74) and a first polysilicon film (FIG. 23(A):

70) on the entire circuit and then patterning the tunnel oxide film 74 and the first polysilicon film 70 so that the tunnel oxide film 74 and the first polysilicon film 70 can only remain in a give region of the cell region, thus defining a floating gate (FIG. 23(C): 14); forming an insulating film (FIG. 23(B): 80) on the entire structure and forming a second polysilicon film (FIG. 23(B): 71) on the insulating film 80; patterning the second polysilicon film 71 and the insulating film 80 so that they can remain only in a given region of the cell region and the peripheral circuit region, thus forming a control gate (FIG. 23(C): 7) on the insulating film (FIG. 23(C): 15) covering the floating gate 14 in the cell region and a gate (FIG. 23(C): 4) on the insulating film (FIG. 23(C): 13) covering a surface of the substrate (FIG. 23(A): 20) in the peripheral circuit region; and performing an impurity ion implantation process for a give region of the semiconductor substrate 20 to form a source region (FIG. 23 (C): 2) and a drain region (FIG. 23(C): 1), so that a flash memory cell is formed in the cell region, and a code address memory cell is formed in the peripheral circuit region (col. 4, lines 5-26 and FIGS. 23(A)-(D)).

Nakajima does not explicitly disclose forming an insulating film including an oxide film and a nitride film on the entire structure and forming a second polysilicon film on the insulating film as recited in present independent claim 7.

Osari, however, discloses forming an insulating film (FIG. 2B: 22) including an oxide film and a nitride film (ONO) on the entire structure and forming a second polysilicon film (FIG. 2D; 26) on the insulating film (col. 7, line 46 to col. 8, line 21 and FIGS. 2A-D). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nakajima and Osari to

enable the insulating film including an oxide film and a nitride film on the entire structure of Nakajima to be formed and furthermore to obtain a double layers gate and a single-layer gate with appropriate pattern precision respectively (col. 3, lines 61-64, Nakajima).

In re claims 8 and 10, Nakajima discloses wherein the gate insulating film (ONO layer, constructed by three layers, oxide/nitride/oxide) (**FIGS: 2B: 22**) is formed by stacking at least two or more layers of at least one of the oxide and nitride film (col. 7, line 46 to col. 8, line 21 and **FIGS. 2A-D**).

In re claim 9, Osari discloses wherein the gate insulating film 22 has a thickness of 300 Angstroms (col. 7, lines 47-61).

In re claim 11, Ma et al. (U.S. Patent 5,981,403) provide evidence that the process of forming an insulating film by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film is well-known to one of ordinary skill in the art at the time of the invention was made. Ma et al. disclose an ONON structure includes a first oxide layer 34, a first nitride layer multilayer region 36, a second oxide layer 38 and a second nitride multilayer region 40 (col. 2, lines 12-16 and **FIGS. 1-3**).

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
August 4, 2004



**W. DAVID COLEMAN
PRIMARY EXAMINER**